WHAT IS CLAIMED IS:

1. A method for processing a semiconductor topography, comprising:

etching a stack of layers within a single etch chamber, wherein the stack of layers comprises a nitride layer interposed between an anti-reflective layer and an underlying layer; and

introducing a noble gas heavier than helium into said etch chamber during said etching.

2. The method of claim 1, wherein said introducing comprises introducing the noble gas during said etching of the anti-reflective layer and of the nitride layer.

3. The method of claim 2, wherein said introducing further comprises introducing the noble gas during said etching of the underlying layer.

4. The method of claim 1, wherein said noble gas comprises argon.

5. The method of claim 1, wherein said nitride layer comprises silicon nitride.

6. The method of claim 1, wherein said anti-reflective layer comprises organic materials.

7. The method of claim 6, wherein said underlying layer comprises a material comprising silicon.

8. The method of claim 7, wherein said underlying layer comprises polysilicon.

9. The method of claim 7, wherein said underlying layer comprises monocrystalline silicon.

10. The method of claim 7, wherein said underlying layer comprises silicon-germanium.

11. A method for processing a semiconductor topography, comprising:

etching an anti-reflective layer in a plasma etch chamber designed to etch a material comprising silicon; and

introducing a first noble gas heavier than helium into said etch chamber during said etching the anti-reflective layer.

12. The method of claim 11, further comprising:

etching a cap layer arranged beneath the anti-reflective layer in the etch chamber; and

introducing a second noble gas heavier than helium into said etch chamber during said etching the nitride layer.

13. The method of claim 12, wherein said cap layer comprises nitride.

14. The method of claim 12, wherein said first and second noble gases are the same.

15. The method of claim 12, further comprising:

patterning a photoresist layer arranged over the anti-reflective layer prior to etching the anti-reflective layer; and

removing remaining portions of the photoresist layer and anti-reflective layer subsequent to said etching the cap layer.

16. The method of claim 12, further comprising etching a lower layer arranged beneath the cap layer in the etch chamber.

17. The method of claim 16, further comprising introducing a third noble gas heavier than helium into said etch chamber during said etching of the lower layer.

18. The method of claim 11, wherein said first noble gas comprises xenon.

19. A method for processing a semiconductor topography comprising introducing a noble gas heavier than helium into an etch chamber during etching of the semiconductor topography such that formation of defects within an etched portion of the semiconductor topography is reduced, wherein said defects comprise bilayer mounds of nitride and a material comprising silicon.

20. The method of claim 19, wherein said defects comprises nitride and polysilicon bilayer mounds.

21. The method of claim 19, wherein said introducing comprises introducing the noble gas into the etch chamber during etching of an anti-reflective layer and a nitride layer of the semiconductor topography.

22. The method of claim 21, wherein said introducing further comprises introducing the noble gas into the etch chamber during etching of a silicon-comprising layer of the semiconductor topography.

23. The method of claim 19, further comprising forming a semiconductor structure within the semiconductor topography, wherein a dimension of said semiconductor structure is within a critical dimension specification.

24. The method of claim 23, wherein said semiconductor structure is a gate structure.

25. The method of claim 23, wherein said semiconductor structure is an interconnect line.

26. The method of claim 23, wherein said semiconductor structure is an isolation region of the semiconductor topography.

27. The method of claim 23, wherein said etch chamber is adapted to form the dimension of the semiconductor structure within said critical dimension specification.